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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/711,748 | 10/01/2004 | Kiran V. Chatty | BUR920040050US1 | 5747 |

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| EXAMINER |
|---|
| KITOV, ZEEV V |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2836 | |

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/711,748 | CHATTY ET AL. | |
| | Examiner | Art Unit | |
| | Zeev Kitov | 2836 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 - 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7 - 11* is/are allowed.

6)☐ Claim(s) *1, 2, 5, 6, 12 - 20* is/are rejected.

7)☒ Claim(s) *3 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on May 30, 2006. Claims 1, 7 and 12 are amended. An Office Action follows.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Andresen et al. (US 6,147,538). Regarding Claim 1, Andresen et al. disclose a transistor network connected between a voltage source and a ground (shown in Fig. 8), a bias network (R3a, R3b in Fig. 8) configured to bias a gate of a first transistor (N1b in Fig. 8) to a portion of a voltage value of the voltage source, and a trigger network (R1, P2, P1a, P1b in Fig. 8) communicating the occurrence of an electrostatic discharge to the gate of the second transistor (N1a in Fig. 3).

Regarding Claim 2, Andresen et al. disclose the first and the second n-FET devices connected in series (N1a, N1b in Fig. 8).

Regarding Claim 5, Andresen et al. disclose the voltage divider (R3a, R3b in Fig. 8) delivering a portion of the supply voltage to the gate of the first transistor (N1b in Fig. 8).

Regarding Claim 6, Andresen et al. disclose the resistor - capacitor circuit (R1, P2 in Fig. 8) filtering out non-electrostatic discharge events from the gate of the second transistor (N1a in Fig. 8).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Regarding Claims 12 - 20, are rejected under 35 U.S.C. 103(a) as being unpatentable over Andresen et al. in view of Lin et al. (US 6,919,602). Regarding Claim 12, Andresen et al. disclose configuring a gate of an upper transistor to be biased to a prescribed value (3.3 volts, col. 9, lines 35 - 39), and coupling an electrostatic discharge event to a gate of a lower transistor (col. 9, lines 15 – 47).

Regarding Claims 13 and 14, Andresen et al. disclose biasing the gate of the upper transistor (3.3 volts, col. 9, lines 35 - 39) with a voltage divider connected between the power rails (unidentified resistor, R3a, R3b in Fig. 8).

Regarding Claims 15 - 17, Andresen et al. disclose biasing the gate of the upper transistor to a prescribed fraction of the voltage of the power supply rail

(divider is formed by unidentified resistor, R3a, R3b in Fig. 8). However, its transistor network is connected to the I/O pin rather than between the power rails. Lin discloses the ESD protection circuit with transistors connected between the power supply rails (Vdd and Vss in Fig.4B). The reference has the same problem solving area, namely providing ESD protection to the semiconductor devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied the Andersen solution to the Lin case, i.e. protecting the semiconductor devices against ESD events on the power supply rails, because such application would expand the market for manufacturers of the Andersen circuit.

Regarding Claims 18, Andresen et al. disclose the high-pass filter communicating with a source and a drain of the lower nFET (N1b in Fig. 8); the high-pass filter is communicating with the source and drain of the lower nFET delivering the signal through transistors (P1a, P1b in Fig. 8) to the drain of the lower nFET and through additional resistor (R3b in Fig. 8) to the gate.

Regarding Claim 20, Andresen et al. disclose configuring the power supply rail to be in communication with a voltage source and the ground voltage (Vdd and ground in Fig. 8).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Andresen et al. As per Claim 19, it differs from Claim 18 rejected above by its limitation of the time constant having specific value of one microsecond. The hi-pass filter is intended to filter out the low frequencies, therefore its time constant,

which is associated with a cut-off frequency of the filter, is a result effective variable. Base on the Court Decision, it would have been obvious to one of ordinary skill in the art at the time the invention was made to set the time constant of the filter to a value of one microsecond, since it has been held that discovering an optimum value of the result effective variable involves only routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

***Allowable Subject Matter***

1. Claims 7 - 11 allowed. A reason for that is that Claim 7 recites series connected the first and the second nFET's, wherein a filter connected to the gate of the lower nFET filtering out low frequency signals between the power supply and the gate of the lower nFET.

2. Claims 3 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. A reason for that is that Claim 3 recites, inter alia, the third nFET connected in series between the first nFET and the second nFET.

***Response to Arguments***

Applicant Arguments have been given careful consideration but they have been found non-convincing.

1. Applicant argues about Examiner's numbering of the claimed the first and the second transistors analogs in the reference. According to him, the N1a

transistor should be identified with the first transistor of the claim and N1b transistor with the second transistor of the claim, while the Examiner identified N1b as the first transistor and N1a as the second. However, there is not any reason to number transistors of the reference according to the Applicant choice. Examiner is not aware of any rule regarding numbering the elements of the reference. The claim language does not indicate relative position of the first and the second transistors in the circuit or interconnection of the transistors to the remainder of the circuit. The Argument is therefore non-convincing.

2. With regard to Applicant allegation about "swapping" transistors and non-functional circuit obtained as a result (pages 13 and 14) the Examiner has never suggested any swap between the transistors.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.
7/30/2006

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